REMARKS

I. STATUS OF THE CLAIMS

Claims 1-25 stand rejected. Claims 23-25 stand objected to. Claims 24 and 25 stand objected to by virtue of their dependency on claim 23. Claim 17 is cancelled; thus, Claims 1-16 and 18-25 are pending.

Claim 23 is amended in response to the Examiner's objection to replace the semicolon at the end of Claim 23 with a period, and to correct a typographical error. The undersigned respectfully requests removal to the objections of Claims 23-25. This amendment does not add new matter.

Claim 1 is amended to essentially incorporate Claim 9 and to correct a typographical error that appeared in as-filed claim 9, namely, "second tests data" is amended to "second test data". Claim 9 is amended to independent form. Support for amended Claim 9 is found in at least Figs. 1D and 2, paragraph **[0053]** of the Written Description, and as-filed claim 1. Claim 10 is amended to independent form, essentially incorporating as-filed Claim 1. Claim 16 is amended to essentially incorporate as-filed Claim 17, which is cancelled. These amendments do not add new matter.

Claim 18 is amended to eliminate redundancy with amended Claim 16. Claim 19 is amended to conform antecedent basis to amended Claim 16. These amendments do not add new matter.

II. REJECTIONS UNDER 35 U.S.C. § 102

Claims 1-10, 13-18, and 20-25 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,024,327 by Dastidar et al. (hereinafter "Dastidar"). Claim 17 is cancelled, rendering its rejection moot.

The Examiner states that Dastidar "teaches a method of isolating a fault on a line segment of a switch matrix comprising (columns 1-2, lines 65-2): generating a first route between an input of the switch matrix and an output of the switch matrix through a first programmable interconnect point (Figure 1 # 121, column 2, lines 10-25) on the line segment and through a first adjacent programmable interconnect point (column 3, lines 32-35); configuring the first route in the switch matrix (column 2, lines 25-30);

applying a first test vector at the input (column 2, lines 30-35); measuring first test data at the output (column 2, lines 30-35); storing the first test data (Figure 1 # 123, column 3, lines 10-25) and at least a portion of the first route (Figure 1 # 113); generating a second route between the input and the output (column 3, lines 25-30) through the first programmable interconnect point on the line segment and through a second adjacent programmable interconnect point (column 3, lines 32-35), configuring the second route in the switch matrix (column 3, lines 25-30); applying a second test vector at the input (column 3, lines 30-32); measuring second test data at the output (column 3, lines 25-36); and storing the second test data and at least a portion of the second route (column 3, lines 25-35). The Applicants respectfully traverse.

Dastidar does not disclose or suggest a method of isolating faults on a line segment of a switch matrix. Dastidar discloses that "[a] series of tests are performed to detect the presence of any manufacturing detects (*sic*) in the programmable logic device" (column 2, lines 3-4). Merely detecting the presence of a manufacturing defect in a device does not indicate where the defect occurs along a line segment, only that the device has a defect somewhere along that path.

The burden of establishing a *prima facie* case of anticipation resides with the Patent and Trademark Office (*In re Skinner*, 2 USPQ2d, 1788, 1788-89 (B.P.A.I. 1986)). The Examiner must rely on the applicants' disclosure to properly determine the meaning of terms used in the claims (*Markman v. Westview Instruments* , 52 F.3d 967, 980, 34 USPQ2d 1321, 1330 (Fed. Cir.) (en banc), aff'd, 116 S. Ct. 1384 (1996)). A *prima face* case of anticipation requires that every aspect of the claimed invention, either explicitly or impliedly, is taught in the cited reference. Any feature not directly taught must be inherently present. If the examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of the patent (*In re Oetiker*, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992)).

Amended Claim 1 recites, among other elements, "evaluating the first test data and the second test data against a layout schematic of a programmable logic device." The claims must be analyzed, not in a vacuum, but always in light of the teachings of the disclosure as it would be interpreted by one of ordinary skill in the art. *In re Angstadt*, 537 F.2d 498, 190 USPQ 214, 217 (C.C.P.A. 1976); *In re Moore*, 439 F.2d

1232, 1235, 169 USPQ 236, 238 (C.C.P.A. 1971). During patent examination, the pending claims must be "given [their] broadest reasonable interpretation consistent with the specification." *In re Hyatt*, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). The broadest reasonable interpretation of the claims must be consistent with the interpretation that those skilled in the art would reach. *In re Cortright*, 165 F.3d 1353, 1359, 49 USPQ2d 1464, 1468 (Fed. Cir. 1999).

Dastidar does not disclose isolating faults on a line segment of a switch matrix. Dastidar applies test vectors to routes to determine if the interconnects and circuit functions are operable (Abstract). Dastidar discloses using a connectivity graph for developing routes that are combined into configuration patterns. A connectivity graph represents the interconnections on a programmable integrated circuit as nodes. A router automatically generates tests routes that connect the nodes in the connectivity graph between control points and observation points on the programmable integrated circuit. The routes are grouped into configuration patterns that can be tested in one test cycle. Test vectors are then applied to the routes to determine if interconnections and functions on the programmable circuit are operable. (Col. 1, lines 32-40, see also, Col. 4, lines 4-25).

Dastidar does not teach or suggest evaluating the first test data and the second test data against a layout schematic of a programmable logic device. A connectivity graph is not a layout schematic. The words "layout" or "schematic" do not even appear in Dastidar. Therefore, Claim 1 and all claims that depend from Claim 1 are patentable.

Claim 6, which depends from Claim 1, recites that the second test vector is the same as the first test vector. The Examiner cites Col. 3, lines 55-65 of Dastidar in the rejection of claim 6. This section refers to development of a test plan using a simulator (see Fig. 2), not to applying test vectors to the input of a switch matrix. Dastidar must be considered as a whole. In Col. 3, lines 47-49, Dastidar states that "[e]ach configuration file can hook up a plurality of non-overlapping routes that can be simultaneously connected on the PLD and tested in one cycle."

The "second route" in Claim 1, from which Claim 6 depends, is "through the first programmable interconnect point on the line segment". In Col. 5, lines 11-13, 17-19,

and 22-24, Dastidar emphasizes that each node used in one route is not used in another. In Col. 5, line 28, Dastidar again states that the router 302 makes non-overlapping routes. In Col. 6, lines 6-8, Dastidar states that "ATPG vector generator 305 creates functional vectors 306 for each configuration pattern 304", and in Col. 6, lines 60-61, that "[t]he functional vectors are tailored specifically for each of the routes in the configuration files". Dastidar does not disclose or suggest using the same test vector for the first and second routes, and, when considered as a whole, teaches away from claim 6. Claim 6 is further patentable.

Amended Claim 9 defines "[a] method of locating a fault on a failed line segment of a switch matrix" and recites, among other elements, "comparing the first test data and the second test data against a layout schematic of a programmable logic device so as to locate the fault on the failed line segment".

Dastidar does not disclose or suggest locating faults on a failed line segment of a switch matrix. Dastidar applies test vectors to routes to determine if the interconnects and circuit functions are operable (Abstract). Dastidar discloses using a connectivity graph for developing routes that are combined into configuration patterns. A connectivity graph represents the interconnections on a programmable integrated circuit as nodes. A router automatically generates tests routes that connect the nodes in the connectivity graph between control points and observation points on the programmable integrated circuit. The routes are grouped into configuration patterns that can be tested in one test cycle. Test vectors are then applied to the routes to determine if interconnections and functions on the programmable circuit are operable. (Col. 1, lines 32-40, see also, Col. 4, lines 4-25).

Dastidar does not teach or suggest comparing the first test data and the second test data against a layout schematic of a programmable logic device. A connectivity graph is not a layout schematic. Dastidar does not teach or suggest claim 9, and claim 9 is patentable.

Amended Claim 10 recites, among other elements, "applying a first test vector at the input, the first test vector comprising a first series of first digital test values followed by a second series of second digital test values followed by a third series of the first digital test values". The Examiner cites Col. 6, lines 1-20 in rejecting claim 10.

Col. 6, lines 14-20 of Dastidar disclose a single test value of 1 providing a read value of 0 in a route using only one inversion. The single test value disclosed in Dastidar is not a first series of first digital test values. One following the disclosure of Dastidar would not be led to apply a first test vector at the input, the first test vector comprising a first series of first digital test values followed by a second series of second digital test values followed by a third series of the first digital test values. Claim 10 and all claims that depend from claim 10 are patentable.

Claim 14 recites, among other elements,

"(c) generating a first route through a first port of the switch matrix to an Nth original PIP where N is an integer;

(d) adding a second route from the Nth original PIP to an Mth adjacent PIP where M is a second integer;

(e) adding a third route from the adjacent PIP to a second port of the switch matrix;

(f) storing a route including the first route, second route, and third route in a route directory

(g) repeating steps (d), (e) and (f) for all adjacent PIPs adjacent to the original PIP;

(h) repeating steps (c), (d), (e), (f) and (g) for all original PIPs".

The Examiner recites various portions of Dastidar against various elements of Claim 14. The Applicants respectfully traverse the Examiner's position. For example, the Examiner cites Dastidar, Col. 3, lines 25-35 against step (f) storing a route including the first route, second route, and third route in a route directory and Col. 3, lines 25-35 against step (g) repeating steps (d), (e) and (f) for all adjacent PIPs adjacent to the original PIP.

In Col. 3, lines 25-36, Dastidar discloses using a simulator to test software representing a PLD to determine if the test vectors are accurate. In Col. 3, lines 47-49, Dastidar discloses that "[e]ach configuration file can hook up a plurality of non-overlapping routes that can be simultaneously connected on the PLD and tested in one test cycle." This teaches away from step (g) of Claim 14 because the routes stored in repeated step (f) include overlapping portions. Dastidar further states that

"[a] dead end is a node in which all of its programmable fan-out connections have already been used. There is no way out of a dead end except to back out of it. When router 302 hits a dead end, it backs out of the dead end node and continues the route to an observation point along another path." (Col. 5, lines 37-32). This suggests that that route having a node in which all of its programmable fan-out connections have been used is not included in the test cycle of Dastidar, which also teaches away from step (g) of claim 14.

Dastidar is directed at techniques for generating non-overlapping routes that may be concurrently tested in a single test cycle (Abstract, Col. 7, line 20, Claim 1). Dastidar must be considered as a whole. Restricting routes in a test cycle to nodes that are not used more than once in any test cycle would not result in claim 14. Dastidar does not disclose or suggest Claim 14, and Claim 14 is patentable.

Claim 15 defines "[a] system of isolating a fault on a line segment of a switch matrix" and recites, among other elements, "means for generating routes between an input of the line segment and an output of the line segment through each of the original programmable interconnect points and through each of the programmable interconnect points adjacent to each of the original programmable interconnect points". Dastidar does not teach or suggest this because Dastidar avoids using a node in more than one route in a test cycle, so that multiple routes may be simultaneously tested in a test cycle. The techniques disclosed in Dastidar only indicate whether a route is operable, Dastidar does not teach a system of isolating a fault on a line segment of a switch matrix. Therefore, claim 15 is patentable.

Amended Claim 16 recites, among other elements, "a failure analysis software module stored in the memory and configured to receive test results related to the line segment from the tester and to perform fault isolation analysis on the received test results." The term "fault isolation" must be interpreted in light of the Applicants disclosure and must be consistent with the interpretation that those skilled in the art would reach.

Following the disclosure of Dastidar would not identify the physical point(s) of failure in a line segment of a device. Contrary to the Examiner's assertion, Col. 9, lines 12-15 of Dastidar does not disclose or suggest performing fault isolation analysis.

These lines of Dastidar merely say "[t]he computer system according to claim 8 further comprising: code for testing the programmable circuit elements using the test pattern by applying test values to control points and reading output values from observation points." There is no mention or suggestion that fault isolation analysis is performed. Claim 16 and all claims that depend from claim 16 are allowable.

Claim 23 recites, among other elements, "identifying an original programmable interconnection point on the line segment having a fault" and "generating a route between an input of the line segment and an output of the line segment through the original programmable interconnection point and through the output programmable interconnection point."

The Examiner cites Dastidar, Col. 4, lines 1-11 and lines 43-46 against these elements of claim 23. In Col. 4, lines 1-11, Dastidar discloses using a connectivity graph of the IC. Lines 43-46 of Col. 4 state that "[a]fter a connectivity graph for a programmable circuit has been created and stored in a database 301, an automatic test program generator (ATPG) router 302 automatically creates a series of routes across the programmable circuit." There is no disclosure or suggestion in Dastidar of identifying an original programmable interconnection point on the line segment having a fault.

Referring to Fig. 3 of Dastidar, it is seen that route generation and simulator-based test vector verification occur prior to testing a physical device. Thus, no failed line segment has been identified when the routes are generated, and Dastidar does not identify an original programmable interconnection point on the line segment having a fault. Dastidar does not disclose or suggest claim 23, and claim 23 and all claims that depend from claim 23 are allowable.

Claim 25, which depends from Claim 23 through Claim 24, further recites "testing the generated route on the line segment in the integrated circuit (IC) to produce a test result . . . and analyzing the test result to determine a location of the fault." As argued above in support of Claim 23, Dastidar does not disclose or suggest testing a route generated after identifying an original PIP in a faulty line segment. Dastidar generates routes, and then tests the device. Dastidar does not disclose or

suggest analyzing a test result to determine the location of a fault. Therefore, Claim 25 is further patentable.

III. REJECTIONS UNDER 35 U.S.C. § 103

Claims 11, 12, and 19 stand rejected as being unpatentable over Dastidar.

Claim 11, which depends from claim 10, recites that "there are at least three first digital test values in the first series." The Examiner urges that, since Dastidar "is already using functional digital test data vectors to test the device", that "it would be obvious to represent them with three different digital test values". The Applicants respectfully traverse. Claim 11 does not recite three different digital test values, but rather a test vector having a first series of a first digital test value. In other words, the test vector includes a 1-1-1 series or a 0-0-0 series.

The Examiner provides no motivation or convincing line of reasoning why Dastidar would lead one to use at least three first digital test values in a first series of a test vector of a functional test vector. In Col. 6, lines 14-20, Dastidar provides an example of a single test value, and thus teaches away from a first series of at least three first digital values. The Examiner notes that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum range or workable range involves only routine skill in the art, citing *In re Aller*, 105 USPQ 233. However, a particular parameter must first be recognized as a result - effective variable, *i.e.*, a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. *In re Antonie* , 559 F.2d 618, 195 USPQ 6 (CCPA 1977). The Examiner does not indicate where the "general conditions" of claim 11 are found in the prior art, or what recognized result is disclosed in Dastidar that would lead one to make the urged modification. Dastidar does not recognize any result or suggest any motivation for having at least three first digital test values in a first series. No *prima facie* case of obviousness has been established.

Dastidar discloses using a vector generator to generate test values for verification of proper operation of a PLD, and uses a simulator to determine if the test vectors are accurate (Col. 3, lines 16-25). A simulator does not have manufacturing

defects or variations that arise in physical devices, and Dastidar does not teach or suggest why a series of three first digital values would be desirable when developing test vectors to be verified in a simulator, or that the vector generator would produce a test vector having such a series. Dastidar does not teach or suggest Claim 11, and Claim 11 is further patentable.

Claim 12, which depends from Claim 11, recites that "there are at least three second digital test values in the second series." Dastidar does not teach or suggest a test vector having a first series of first digital test values followed by a second series of second digital test values, and thus cannot teach or suggest that there are at least three second digital test values in the second series. Claim 12 is further patentable.

Amended claim 19, which depends from Claim 16 through Claim 18, further recites that "information used by the tester from the test input file is modified based on feedback from the failure analysis software module." The Examiner acknowledges that Dastidar does not teach such a system, and urges that it would have been obvious "to modify the test input file based on feedback from the failure analysis module . . . because doing so would enable Dastidar et al.'s invention to cross check for a diverse number of errors."

As argued in support of Claim 16, the Examiner has not identified a failure analysis module in Dastidar. The Examiner's motivation appears, at best, to be hindsight reasoning because it is the Applicants who teach the desirability of modifying the test input file based on feedback from a failure analysis module. A claim is not obvious when the suggestion to modify comes from the Applicants' disclosure. Dastidar, which must be considered as a whole, suggests a line of development that diverges, and thus teaches away from, claim 19.

Dastidar groups routes into configuration patterns that can be tested in one test cycle (Abstract). Dastidar generates test vectors and runs the test vectors and configuration files on a simulator before testing an actual PLD (Col. 3, lines 10-42). The modification urged by the Examiner appears contrary to Dastidar's goal of testing all routes in a test pattern in a single test cycle because it would invoke another test development cycle after the physical device had been tested the first time. Furthermore, a change in a route in the test input file might violate Dastidar's stated

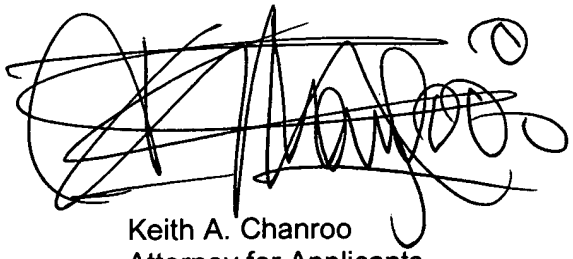
goal of being able to test all routes of a configuration pattern in a single test cycle because the modified test input file might include a node used in another route in that test pattern. Having to re-confirm that the modified test input file did not violate the non-overlapping route condition would require substantial redesign of Dastidar's method and confound the single-cycle test efficiency that Dastidar strives for.

Dastidar does not disclose a failure analysis software module and therefore does not disclose all elements of claim 19. Without a failure analysis software module, there cannot be a feedback path to the tester from a failure analysis software module. The Examiner is creating prior art that is simply not there. The urged modification would require a substantial redesign of the technique of Dastidar. Claim 19 is not obvious and is further patentable.

CONCLUSION

The Applicants submit that all claims are now in condition for allowance. Favorable reconsideration and timely issuance of a Notice of Allowance are respectfully requested. Should the Examiner consider necessary or desirable any formal changes anywhere in the specification, claims, and/or drawings, then it is respectfully asked that such changes be made by an examiner's amendment, if the Examiner feels this would facilitate passage of the case to issuance. If the Examiner believes a telephone conference would expedite prosecution of this application, the Examiner is cordially invited to telephone the undersigned at (408) 879-4984.

Respectfully Submitted,



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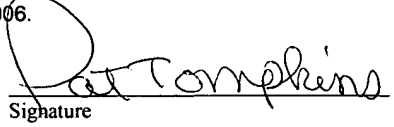

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